Abstract of the Disclosure

A technique is provided for implementing device/chip outputs protection during JTAG circuit board testing. A protection circuit detects a short or overload on every output pin; and within a short time (i.e. 1 clock cycle) disables the output-enable signal of the associated output buffer only during tests using the JTAG circuitry (IEEE 1149.1). A protection register is connected to the TAP controller for analysis to point to the exact failure location.